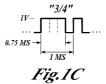


Fig.1A



Fig.1B



NUMBER OF UNIT PULSE LENGTHS	MODULATOR BINARY OUTPUT COMBINATIONS	TIMER STATE	EFFECTIVE DUTY CYCLE
0	0 0 0 0 0 0 0 0	0 1 0 1	= 0% (0/8)
1	0 0 0 1 0 1 0 0	0 1 0 1	= 12.5% (1/8)
2	0 I 0 I 0 I 0 I 0 I 1 0 1 0	0 1 0 1 0 1	= 25% (2/8 = 1/4)
3	0 0 0 1 1 1 0 0 1 1 0 0 1	0 1 0 1 0 1	= 37.5% (3/8)
4	0 I 1 I 1 I 0 I 1 0 1 0 1 0	0 1 0 1 0 1	= 50% (4/8 = 1/2)
5	1 0 1 1 1 1 1 0	0 1 0 1	= 62.5% (5/8)
6	1 1 1 1 1 1 1 1	0 1 0 1	= 75% (6/8 = 3/4)

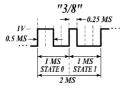


Fig.3A

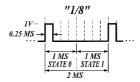


Fig.3B

DUTY CYCLE	POSSIBLE MODULATOR BINARY OUTPUT COMBINATIONS	TIMER STATE
0% (0/8)	0 0	0
12.5% (1/8) 25% (2/8)	0 1 0 0 0 0	0 1
	0 1	0
	1 0 1 0 0 0	0
	0 1 0 1	0
37.5% (3/8)	0 0 1 1	0 1
	1 1 0 0	0 1
	0 1 1 0	0
	1 0 0 1	0 1
50% (4/8)	0 0 1*00 1*00	1
	0 0	0 1 0
	11	1 0
	0 1	1 0
	1 0	1 0
62.5% (5/8) 75% (6/8)	1* 00 1* 00	0
	0 1	1 0
	1 0	0
	1 1 1* 00	0
	1 0	0
	1 * 00 1 1 1 1	0 1
87.5% (7/8)	1 1 1* 00 1 1	0
	1 I 1* 00	0
100% (8/8)	1* 00 1* 00	0

Fig.4





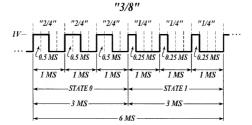
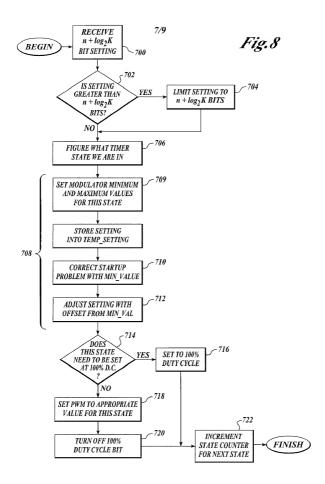


Fig. 6

## 

PWM PERIOD = 2 MS, TIMER PERIOD = 5 MS

Fig. 7



TOTAL PULSE	MODULATOR OUTPUT IN EACH TIMER STATE								
DURATION AS MEASURED IN UNIT	TIMER STATE								
PULSE LENGTHS	1	2	3	4	5	6	7	8	
0	0	0	0	0	0	0	0	0	
1	1	0	0	0	0	0	0	0	
2	1	0	0	0	1	0	0	0	
3	1	0	1	0	1	0	0	0	
4	1	0	1	0	1	0	1	0	
5	1	1	1	0	1	0	1	0	
6	1	1	1	0	1	1	1	0	
7	1	1	1	1	1	1	1	0	
8	1	1	1	1	1	1	1	1	
9	2	1	1	1	1	1	1	1	
10	2	1	1	1	2	1	1	1	
11	2	1	2	1	2	1	1	1	
12	2	1	2	1	2	1	2	1	
13	2	2	2	1	2	1	2	1	
14	2	2	2	1	2	2	2	1	
15	2	2	2	2	2	2	2	1	
16	2	2	2	2	2	2	2	2	
17	3	2	2	2	2	2	2	2	
18	3	2	2	2	3	2	2	2	
19	3	2	3	2	3	2	2	2	
20	3	2	3	2	3	2	3	2	
21	3	3	3	2	3	2	3	2	
22	3	3	3	2	3	3	3	2	
23	3	3	3	3	3	3	3	2	
24	3	3	3	3	3	3	3	3	
•	_	•	•						
		:	:	:	:	:	:	:	
2040	255	255	255	255	255	255	255	255	
:	:	:	:	:	:	:	:	:	
2047	256	256	256	256	256	256	256	256	

Fig.9

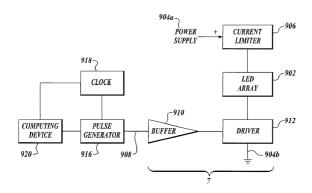


Fig.10